

IN THE CLAIMS:

1. A flash memory comprising:
an array of non-volatile memory cells;
data connections;
an interconnect configuration compatible with a rambus dynamic random access memory (RDRAM); and
output circuitry to provide output data on the data connections on rising and falling edges of a clock signal.
2. The flash memory of claim 1 further comprising sense amplifier circuitry coupled to the array, wherein the sense amplifier circuitry detects a differential voltage.
3. The flash memory of claim 1 further comprising input circuitry to receive input data on the data connection on rising and falling edges of a clock signal.
4. A flash memory comprising:
an array of non-volatile memory cells;
data connections;
a clock signal connection to receive a clock signal;
an interconnect configuration compatible with a rambus dynamic random access memory (RDRAM);
output circuitry to provide output data on the data connections on rising and falling edges of the clock signal; and
input circuitry to receive input data on the data connections on rising and falling edges of the clock signal.

5. A flash memory comprising:
 - an array of non-volatile memory cells, wherein the array comprises bit lines couplable to the non-volatile memory cells;
 - sense amplifier circuitry coupled to the bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines;
 - pre-charge circuitry coupled to pre-charge the bit lines to first and second voltage levels to provide an initial differential voltage prior to sensing a memory cell;
 - data connections;
 - a clock signal connection to receive a clock signal;
 - an interconnect configuration compatible with a rambus dynamic random access memory (RDRAM); and
 - output circuitry to provide output data on the data connection on rising and falling edges of the clock signal.
6. The flash memory of claim 5 further comprising input circuitry to receive input data on the data connection on rising and falling edges of the clock signal.
7. A flash memory comprising:
 - an array of non-volatile memory cells;
 - data connections;
 - a clock signal connection to receive a clock signal;
 - an interconnect configuration compatible with a rambus dynamic random access memory (RDRAM); and
 - control circuitry coupled to the array to provide two data access operations per clock cycle.
8. A method of reading a flash memory comprising:
 - providing a read command;
 - providing memory cell addresses;

reading first and second data words from non-volatile memory cells;
outputting the first data word on a rising edge of a clock signal following a rambus dynamic random access memory (RDRAM) compatible format; and
outputting the second data word on the falling edge of the clock signal following the rambus dynamic random access memory (RDRAM) compatible format.

9. The method of claim 8 wherein the non-volatile memory cells are floating gate memory cells and the comparator circuit detects a voltage of a word line coupled to non-volatile memory cells.
10. A method of reading a flash memory comprising:
 - reading first and second data words from non-volatile memory cells;
 - outputting the first data word on a rising edge of a clock signal following a rambus dynamic random access memory (RDRAM) compatible format; and
 - outputting the second data word on the falling edge of the clock signal following the rambus dynamic random access memory (RDRAM) compatible format.
11. A processing system comprising:
 - a processor; and
 - an RDRAM compatible flash memory coupled to the processor comprising:
 - an array of non-volatile memory cells;
 - a clock signal connection to receive a clock signal; andcontrol circuitry coupled to the array to provide two data access operations per clock cycle following a RDRAM compatible format.
12. A processing system comprising:
 - a processor;
 - a single communication bus coupled to the processor;
 - a volatile memory device coupled to the single communication bus; and

